Comparison of 3-bit per cell NAND Flash Memories

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Executive Summary

The following is a summary of the key takeaways of this report.

- *To improve reliability and performance, SanDisk/Toshiba have implemented the XXXXXXXXXX for the NAND flash devices. Hynix and Samsung continue to employ the XXXXXXXXXXXXXXX.*
- *The XXXXXXXXXXX may face scaling challenges for future generations of NAND flash memories.*
- *Three-bit per cell endurance and retention are much lower than comparable MLC devices with retention XXXXXXXXX being the norm.*
- *Programming speed for 3-bit per cell devices is slower than MLC devices due to the increasing of the number of verify levels and the ISSPP reduction. Various algorithms have been implemented to meliorate the performance degradation.*
- *The cell efficiency of the SanDisk/Toshiba and Hynix devices are XXXXXXXXXXXXXX whereas Samsung's first generation product is relatively XXXXXXXXXXXXXX.*
- *The Samsung 3-bit per cell device's specified endurance is surprisingly XXXXXXXXXXX compared to SanDisk/Toshiba or Hynix's.*

Summary

Table 6 provides a comparison of the SanDisk/Toshiba, Hynix and Samsung 3-bit per cell NAND flash memory products. A variety of algorithms were implemented to improve the programming throughput.

From a design layout point of view, XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX.

Both endurance and retention are XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX.

Hynix has chosen to improve the endurance of its devices with XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

Table 6 Key Parameters Comparison

Features	*SanDisk/ Toshiba 16Gb*	*Hynix 32Gb*	*SanDisk/ Toshiba 32Gb*	*Samsung 16Gb*
Volume production				
Technology				
Size				
Unit cell size (μm^2/bit)				
Cell efficiency				
Gb/mm^2				
Page/plane				
Planes				
Blocks/plane				
Block size				
String				
Pages/block				
Architecture				
Number of Page Buffers				
Page Buffer Organization				
Die Size				
X Y device size				

Features	*SanDisk/ Toshiba 16Gb*	*Hynix 32Gb*	*SanDisk/ Toshiba 32Gb*	*Samsung 16Gb*
X Y plane size				
Pgm Speed				
Pgm Speed Features				
No. of latches/ Page Buffer				
Row Decoder				
I/O mode				
t_{RC} (min.) / t_{WC} (min.)				
t_R (max.)				
t_{prog} (typ.)				
t_{ers} (typ.)				
ECC				
Endurance				
Retention				

*Forward Insights estimates

Tables 6-10 provides an overview of some of the key technical features of the 3-bit per cell NAND flash memory devices from SanDisk/Toshiba, Hynix and Samsung as well as the advantages and disadvantages of each implementation.

Table 7 Key Features and Advantages & Disadvantages of SanDisk/Toshiba 56nm 16Gb 3-bit/cell NAND Flash Memory

SanDisk/Toshiba 56nm 16Gb 3-bit/cell NAND Flash Memory	
Key Features	*Main Pros/Cons*
	✗
	✓
	✓
	✓

Table 8 Key Features and Advantages & Disadvantages of Hynix 48nm 32Gb 3-bit/cell NAND Flash Memory

Hynix 48nm 32Gb 3-bit/cell NAND Flash Memory	
Key Features	*Main Pros/Cons*
	✗
	✗
	✗
	✗ ✗

Table 9 Key Features and Advantages & Disadvantages of SanDisk/Toshiba 32nm 32Gb 3-bit/cell NAND Flash Memory

SanDisk/Toshiba 32nm 32Gb 3-bit/cell NAND Flash Memory	
Key Features	*Main Pros/Cons*
	✗
	✗
	✗
	✓
	✗

Table 10 Key Features and Advantages & Disadvantages of Samsung 51nm 16Gb 3-bit/cell NAND Flash Memory

Samsung 51nm 16Gb 3-bit/cell NAND Flash Memory	
Key Features	*Main Pros/Cons*
	✗
	✗
	✓

About the Author

Luca Crippa is Senior Technical Analyst for Design Architecture. Luca has more than 10 years of experience in MLC flash memory design. Previously, he was Senior Designer for 48nm floating gate and 36nm floating gate NAND flash memories at Qimonda AG as well as 90nm and 60nm MLC NAND flash products at STMicroelectronics.

He was instrumental in the development of 64Mb, 128Mb and 256Mb MLC NOR flash products at STMicroelectronics and is the author/co-author of 20 U.S. patents and the book *Memories in Wireless Systems* (Springer-Verlag ed., 2008).

Luca received his Bachelors degree at ITIS G. Marconi, Dalmine, Italy in 1992 and a Masters degree in Electronic Engineering at the Politecnico of Milan in 1999. His thesis topic was *Analog circuits design for Multilevel Flash Memory*.

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