Cost and Investment Implications of 3D NAND

Report No. FI-NFL-3DC-0514

Contents

List of Tables

Introduction

The NAND flash industry is on the cusp of a technology inflection point. 2D NAND is reaching its scaling limits with 3D NAND its anointed successor.

In the 2D NAND era, the underlying process technology (with a few exceptions) is essentially the same amongst all the NAND flash manufacturers.

*However, in the 3D NAND era, all the NAND flash manufacturers are developing different 3D NAND concepts with variations in the process implementation. The different processes will impact the investment and manufacturing cost for each of the 3D NAND tech*nologies.

This report provides a detailed analysis of the fab and manufacturing implications of 3D floating gate and charge trap NAND concepts from Samsung, Toshiba, SK Hynix and Intel-Micron versus 16nm 2D NAND. The analysis is based on a bottoms-up process flow analysis for each 3D NAND technology and 16nm 2D NAND.

Some of the questions addressed in this report include:

- *What are the main drivers of the process complexity for 2D NAND and 3D NAND?*
- *What is the tool commonality between 3D NAND and 2D NAND?*
- *What is the cost impact of moving the CMOS under the array in 3D NAND?*
- *How much does it cost to build a Greenfield 3D NAND fab and how does it compare to a 2D NAND fab? What is the equipment footprint required and the breakdown of the investment by process modules?*
- *What is the front end manufacturing cost of a 3D NAND wafer compared to a 2D NAND wafer?*
- *What is the investment required to convert an existing 2D NAND fab to 3D NAND? What is the impact on the fab cycle time and manufacturing capacity?*
- *What is the incremental investment required to transition a 32 layer 3D NAND fab to 64 layers? What is the impact on fab cycle time and manufacturing capacity?*

3D NAND Flash Memory Cell

The most important question with regard to the introduction of 3D NAND flash technologies is what is the most promising memory cell concept? The candidates are the floating gate (FG) and the charge trapping (CT) cell concepts. This single question can be elucidated into two questions, highlighting the most critical issues of the FG and CT cell concepts with regard to their implementation in 3D NAND strings.

- FG-Question 1: How can the very complex FG cell structure possibly be implemented into a 3D NAND array and benefit from the extensive 2D FG NAND experience?
- CT-Question 2: How can a CT cell work reliably in a 3D NAND array when it could never do so in 2D NAND?

These two questions will be answered in this introduction section which is focused on the implementation of FG and CT cells into 3D NAND strings.

Implementation of Floating Gate Cells into 3D NAND Flash Arrays

In the past, floating gate memory cells were used due to its reliable operation on the basis of a long experience over many technology generations.

One very important aspect of the floating gate cell reliability is the way these memory cells are programmed and erased. It is essential that the electrons which are moved during program and erase are solely transferred through the tunnel oxide (TOX) [1]. Every onset of electron transfer through the inter poly dielectric (IPD) will cause even higher tunnel currents flowing through the whole floating gate stack at higher programming levels and will strongly damage and finally destroy the floating gate cells affected.

The concentration of the tunnel currents to TOX requires a concentration of the voltage drop and therefore the electric field to this tunnel dielectric. This field concentration is an essential aspect of floating gate cells with a conducting FG due to an included capacitive voltage divider which cannot be realized in charge trapping cells. It is obtained by a floating gate cell design where the control gate (CG) to floating gate (FG) coupling area and therefore the CG-FG capacitance (C_{CG}) is sufficiently larger than the TOX coupling area and therefore the FG to cell channel capacitance (C_{TOX}) as depicted in Figure 2 (a) and (b).

3D concepts

Overview

The fabrication of the 3D-NAND concepts into the product is very similar. Since the memory array formation is separated from the logic, the CMOS periphery is quite comparable between the concepts. As shown in Figure 31, we offer two concepts of the CMOS integration. On the one hand, we analyzed the conventional CMOS formation besides the memory array. On the other hand, the array saving concept of shifting the CMOS below the array is considered. The area saving capabilities are analyzed in our report *How 3D NAND stacks up*.

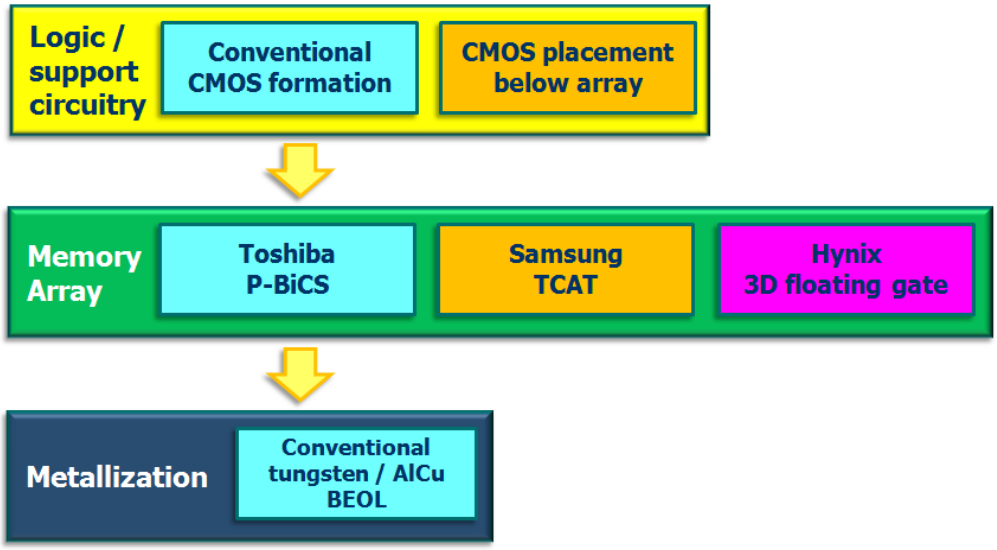

Figure 31. Overview of the 3D NAND concept chapter and the 3D construction kit

Next we introduce the three published concepts of the largest NAND manufacturers, namely, Toshiba p-BiCS, Samsung's TCAT and the 3D floating gate approach of SK Hynix. The 3D NAND construction kit is finalized by the backend of line metallization package, which can be assumed comparable for all concepts.

The die is finalized with the last metal layer and polyimide coating. With the last etch the polyimide is opened called in our case TV (Figure 74).

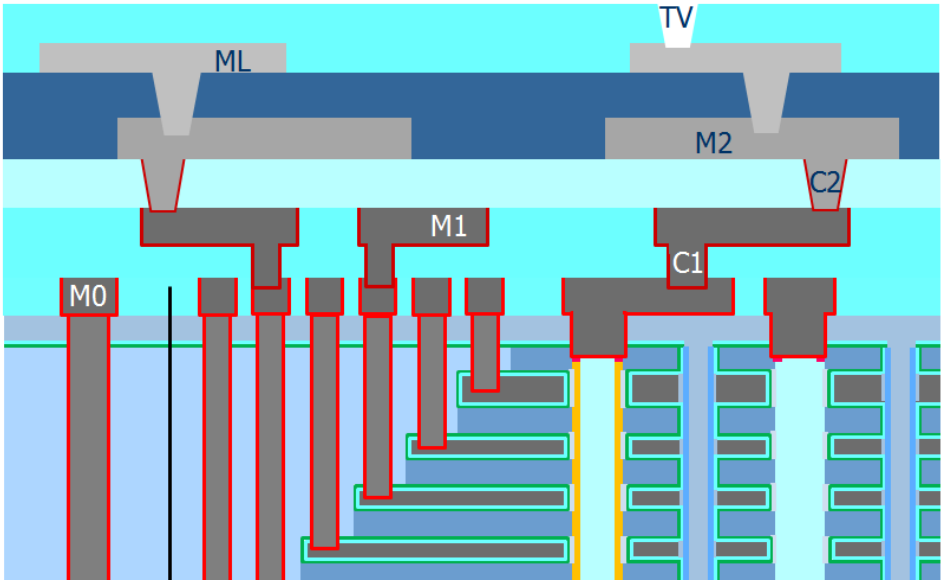

Figure 74. Final BEOL stack after Polyimid deposition and opening showing the used nomenclature in our process proposals

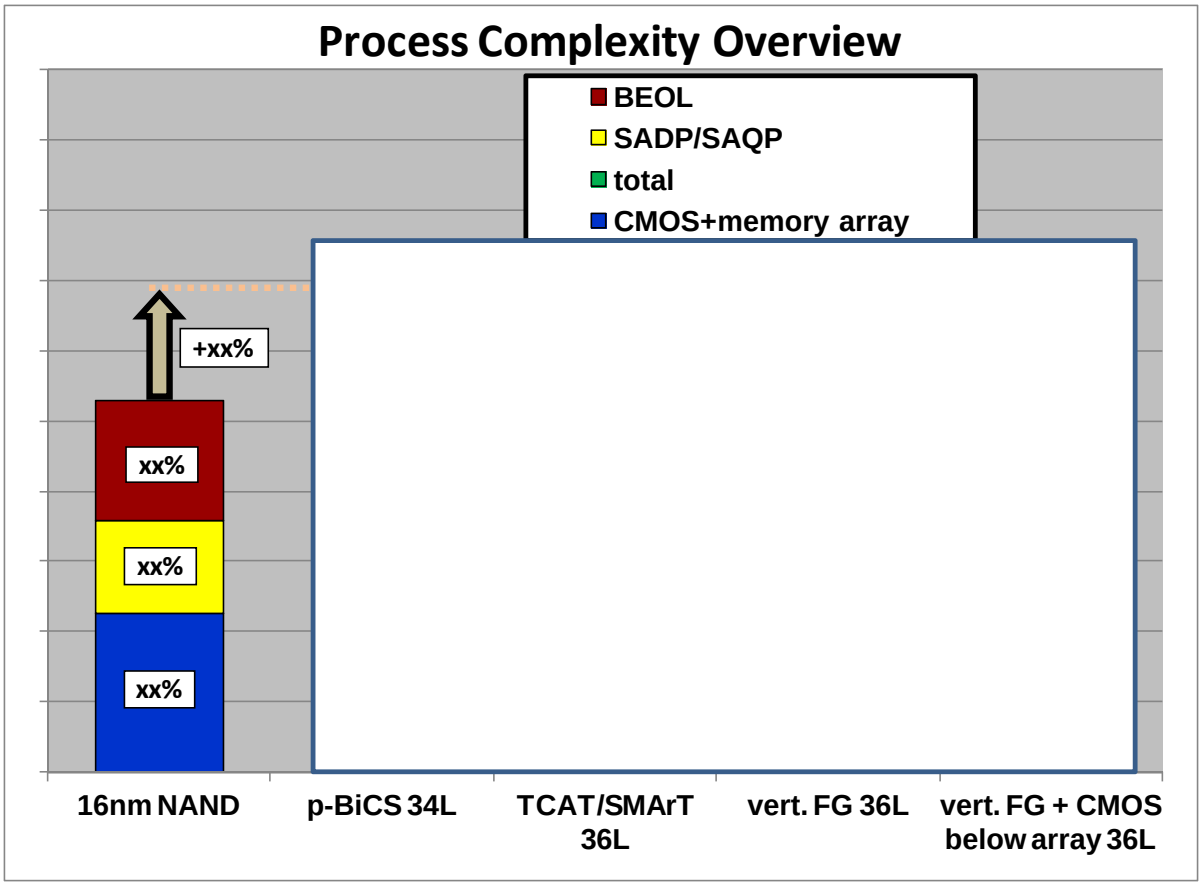

Figure 76. Overview of the key contributors for 16nm NAND process complexity compared to 3D NAND

xxxxx has two contributions which leads to a higher process complexity compared to the competing solutions. Firstly, more process steps are required to xxxxx and xxxxx. Secondly, a xxxxx independent of the xxxxx formation creates an additional overhead of approximately xx% higher process complexity. This is the largest contributor shown in Figure 77 driving the huge gap in process complexity. If both the xxxxx and xxxxx devices require a xxxxx formation, the process complexity for all the concepts will be similar and any differences will be due to the xxxxx formation.

The contribution of the 3D memory array formation to the total process complexity is xxxxx. A relatively large part is driven by the xxxxx, which is needed to xxxxx. This process sequence is highly dependent on xxxxx. For a 32 layer stack, this comes out to about xx% of the total process complexity in the xxxxx.

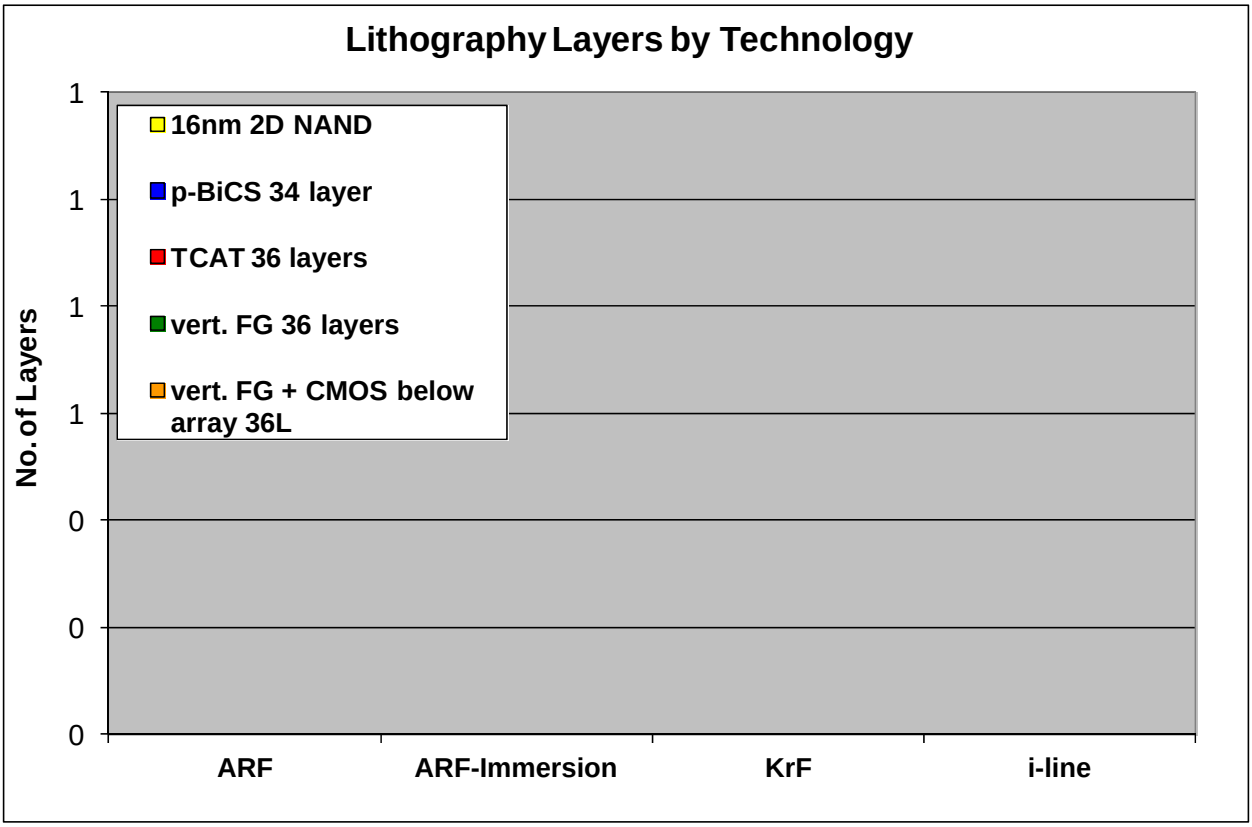

Figure 81. Lithography Layers by Technology

On the other hand, there is a shift from xxxxx to more xxxxx litho steps. This difference can be explained by a different need of xxxxx steps during the fabrication process in case of the 3D NAND concepts.

Next, we give a closer look to the different deposition tools used in our POR proposals in Figure 82. Since the 3D NAND concepts are heavily reliant on deposition, the change for the different deposition techniques is dramatically higher compared to the previously reviewed lithography steps. In the case of xxxxx, the number of process steps is xxxxx for xxxxx. This difference is caused by the fact that the xxxxx are already formed during the multilayer deposition. The other concepts use xxxxx layer as sacrificial material for the xxxxx formation. Hence, the xxxxx CVD tool utilization is tremendously higher compared to 16nm NAND.

The xxxxx of the xxxxx dictates the need for ALD deposition at the key steps. In case of 16nm NAND, we only assume xxxxx the ALD steps for the xxxxx. The 3D NAND concepts need ALD for the xxxxx and additionally to form xxxxx, which are finally separated by xxxxx.

Although the number of xxxxx layers increases in 3D NAND, xxxxx as a proportion of the total equipment investment declines from xx% in 16nm NAND to xx%, xx% and xx% for p-BiCS, TCAT/SMArT and vertical FG respectively due to the xxxxx in 3D NAND.

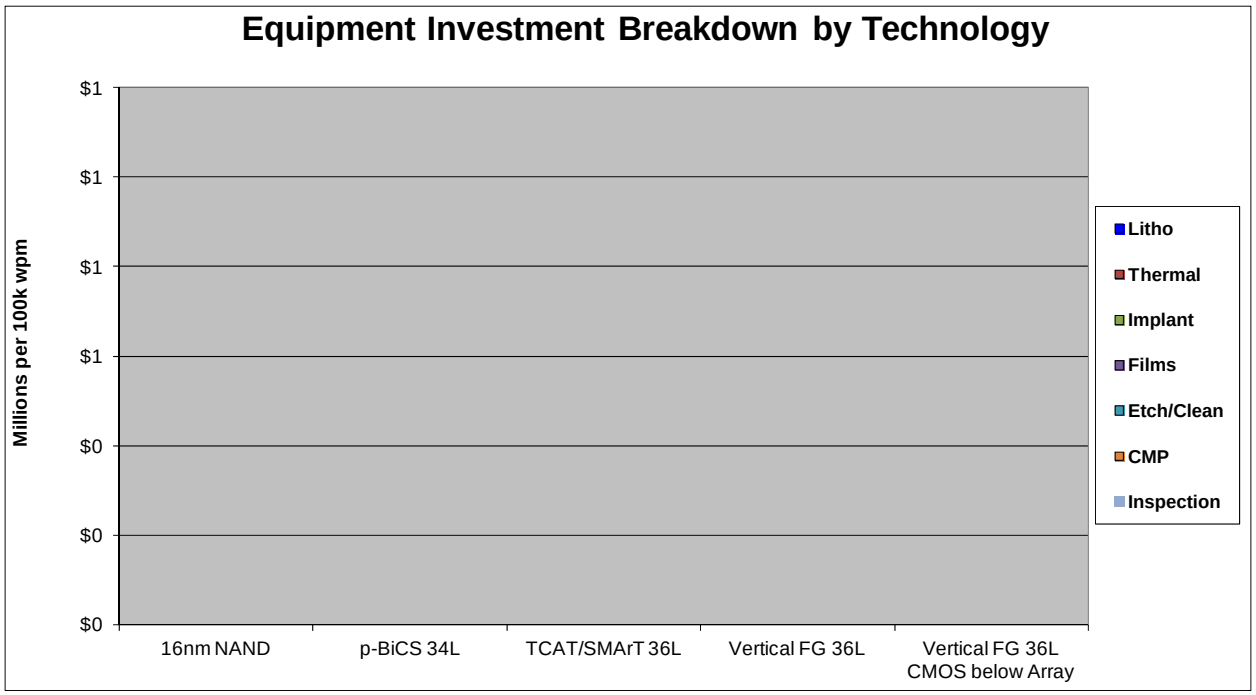

Figure 89. Equipment Investment Breakdown by Technology

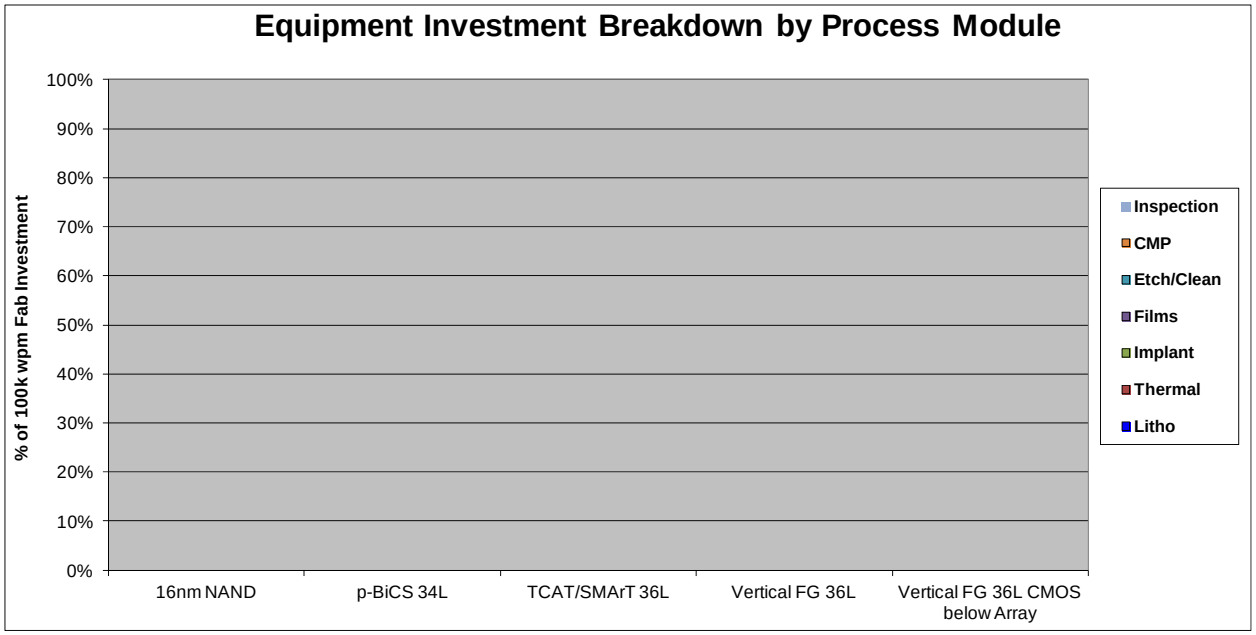

Figure 90. Equipment Investment Breakdown by Process Module

Conversion Costs from 100k wpm 16nm 2D NAND Fab	p-BiCS 34L	TCAT/SMArT 36L	Vertical FG 36L	Vertical FG 36L CMOS below Array
Capacity (k wpm)				
Incremental No. of Tools				
Incremental Equipment Invest ($ m)				
No. of Tools to De-invest				
Equipment De-invest ($ m)				
Eqt Invest by Process Module				
Litho				
Thermal				
Implant				
Films				
Etch/Clean				
CMP				
Inspection				
Eqt De-Invest by Process Module				
Litho				
Thermal				
Implant				
Films				
Etch/Clean				
CMP				
Inspection				
% Increase in No. of Tools by Process Module				
Litho				
Thermal				
Implant				
Films				
Etch/Clean				
CMP				
Inspection				
% Decrease in No. of Tools De-Invested by Process Module				
Litho				
Thermal				
Implant				
Films				
Etch/Clean				
CMP				
Inspection				
Eqt Invest by Process Module % Change				
Litho				
Thermal				
Implant				
Films				
Etch/Clean				
CMP				
Inspection				
Eqt De-Invest by Process Module % Change				
Litho				
Thermal				
Implant				
Films				
Etch/Clean				
CMP				
Inspection				

Table 9. Conversion Costs from 100k wpm 16nm 2D NAND Fab

About the Authors

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He is the author or co-author of more than 30 publications in the field of reliability, degradation characterization, and modeling of future NVM technologies and holds patents in this subject area.

Florian holds a Masters degree in solid state physics and a Ph.D in Electrical Engineering both from the University of Hannover, Germany.

Thomas Melde is at GlobalFoundries Dresden. Previously, he was a Scientist at NaMLab GmbH responsible for charge trap flash device characterization, simulation, and reliability modelling. Thomas' Ph.D. thesis focused on charge trap flash device development at the Flash pre-development team of Infineon/Qimonda, Dresden. He also worked as a research assistant at the Fraunhofer Institute, Division Design Automation, Dresden.

Thomas Melde received his diploma degree in electrical engineering at the Dresden University of Technology, Germany.

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Stefan received a Ph.D. in microelectronics from the Dresden University of Technology, Germany.

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About Forward Insights

Forward Insights provides independent, insightful market research, consulting and information services focusing on semiconductor memories and solid state storage. The company offers unparalleled depth and understanding of the strategic, market and technical complexities of the semiconductor memory landscape.

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