ECC and Signal Processing Technology for Solid State Drives and Multi-bit per cell NAND Flash Memories

2nd edition

Report No. FI-NFL-FSP-0112

Contents

List of Figures

List of Tables

Introduction

In December 2011, it was widely reported that Apple had acquired Anobit Technologies for half a billion dollars. *What prompted Apple to spend that kind of money on a five year old startup?* As the biggest consumer of NAND flash memories, this was clearly a strategic acquisition. The tie-up follows a less widely known acquisition of Storage Genetics by Micron Technology in 2010. Both Anobit and Storage Genetics were developing advanced ECC and signal processing technologies.

As bit errors increase as NAND flash memory scales below 2xnm process technology and transitions to 3-bit per cell architectures, traditional error correction codes such as BCH, RS and Hamming code will no longer be sufficient. These codes suffer from increased overhead in terms of coding redundancy and read latency as the number of errors corrected increases. In addition, the number of electrons stored in the memory cell is decreasing with each generation of flash memory resulting in reduced signal/noise requiring enhanced sensing techniques.

Digital signal processing technology has been employed in the magnetic recording industry since the early 1990's when partial-response maximum-likelihood technology (PRML) was commercialized. DSP technology is now being deployed in 3-bit per cell NAND flash memories and a concerted effort is being made by NAND flash manufacturers and a handful of startups to employ digital signal processing technology to improve the endurance and performance of next generation NAND flash memories and solid state drives. Signal processing technology will be essential for the continued scaling of NAND flash memories.

This research report examines the current state of ECC techniques and explores the technology, roadmap, market, cost and competitive landscape in the flash signal processing space.

About the Authors

Vikas Agrawal was Senior Market Analyst for storage system (SSD/HDD) controllers and markets. His expertise lies in understanding the technology, competitive landscape and market trends for storage components, on-chip and off-chip memory, **storage networking** and **storage system markets.**

Vikas brings 14 years of marketing, business and product development experience from LSI Corp, Texas Instruments, and Integrated Device Technology. In his most recent position, Vikas managed the Emerging Technology start-up business unit at LSI where he was in charge of P&L, strategic planning, business development, product marketing and product management for high performance **Flash/SSD Controllers** and **Flash Channel products.** He was instrumental in driving the start-up division customer base from zero to multiple Consumer and Enterprise OEMs and constructing partnerships with major Flash Manufacturers.

Vikas received his MBA from Southern Methodist University, Dallas in 2002 and Masters in Electrical Engineering from Arizona State University in 1995. He holds six memory-related patents for networking, digital signal processors and wireless products.

Roberto Ravasio was Senior Technical Analyst for DSP, Flash Algorithms and ECC. Roberto has 15 years of experience in **MLC NAND** and **NOR flash design, algorithms** and **hardware for digital signal processing, wireless base band channels** and **error correction codes.** Previously, Roberto was team leader for the design of the 16Gb 36nm floating gate NAND flash memory at Qimonda AG where he was responsible for the architecture definition of the device including matrix organization and device floor plan, HV circuits hierarchical control, ECC and redundancy, embedded controller and compiler, embedded RAM, ROM and Fuse-ROM, DFT custom structure, ONFI Command Interface, high-speed data path, logic design and integration (Front End) and VHDL full chip modeling for recursive test. He also contributed to the development of the MLC algorithm for 48nm NAND flash memory.

Roberto was also team leader of 60nm and 90nm MLC NAND flash products and 0.13µm and 0.18µm NOR flash products at STMicroelectronics.

He is the author/co-author of 25 U.S. patents and the following books: **Error Correction Codes for Non-Volatile Memories, Memories in Wireless Systems** and **VLSI-Design of Non-Volatile Memories.**

Roberto received his Masters degree in Electronic Engineering at the Polytechnic of Milan in 1996.

Gregory Wong is Founder and Principal Analyst. Greg has in-depth knowledge of the cost, performance and markets and applications of **2-bit per cell NOR, NROM**and **NAND flash, 3-bit per cell and 4-bit per cell NAND**and **4-bit per cell NROM flash technologies** as well as **solid state drives**. He also tracks wafer capacity and NAND and SSD shipments.

Greg has 11 years of management experience in strategic planning, business development, competitive intelligence and engineering at Hitachi, Siemens, ProMOS and Qimonda/Infineon. In these positions, Greg was responsible for analyzing and evaluating flash memory vendors' strategies, process technologies, design architectures, product performance, manufacturing capabilities and costs. Greg worked closely with senior management on strategy formulation and setting operational performance targets. He has worked in Canada, Japan, China, Taiwan and Germany.

Greg earned his B.A.Sc. degree in Electrical Engineering from the University of Toronto, and his M.B.A. degree from the Richard Ivey School of Business in London, Ontario.

About Forward Insights

Forward Insights provides independent, insightful market research, consulting and information services focusing on semiconductor memories and solid state storage. The company offers unparalleled depth and understanding of the strategic, market and technical complexities of the semiconductor memory landscape.

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Forward Insights is the only firm that can offer in-depth technical insights and analyses in addition to market insights.

Report Offerings

Forward Insights provides in-depth market and technical intelligence for semiconductor memories, solid state storage and emerging memory technologies. Below is list of some of the reports published by Forward Insights.

NAND Quarterly Insights

NAND Quarterly Insights is a market supply-demand forecast published four times a year which includes vendor shipments, wafer capacity, capex, roadmaps and application forecasts.

SSD Quarterly Insights

SSD Quarterly Insights is a SSD market forecast published four times a year which includes shipment and capacity data for enterprise and client computing applications.

Low Density SLC NAND Flash Memory in Embedded Applications

In last decade, the NAND flash market has witnessed tremendous growth with revenues increasing from $370 million in 2000 to over $20 billion in 2010.

Continuous price declines for NAND flash memory have enabled it diversify beyond removable storage applications to consumer, industrial and computing applications, each with its own specific requirements in terms of performance, features and density.

Since 2006, MLC technology has become mainstream with SLC technology occupying a sliver of the total market. SLC technology is favored in applications requiring high performance, high reliability and wide operating temperatures. Other than the solid state computing and mobile application markets, SLC devices can be found in embedded applications. In particular, low density SLC NAND devices ranging from 128Mb to 4Gb are employed in a variety of consumer and industrial applications.

Due to the higher margin profile of SLC NAND products, NAND flash manufacturers as well as new entrants looking to extend their product portfolios from the NOR flash memory space are all eyeing the low density SLC market.

Low Density SLC NAND Flash Memory in Embedded Applications examines the competition between low density SLC NAND flash, parallel NOR flash and serial flash and sheds light on some of the application drivers for SLC NAND flash memory in the embedded space.

NAND Flash Memory Architecture and Periphery Trends

Analyzes the NAND flash architectural choices affecting the competitiveness of the die area including no. of planes, page buffer layout, interleaved and All Bitline sensing, page size, cell string size, SLC/MLC/8LC/16LC, cell size, wordline fanout, bitlines, ECC and periphery transistors. An examination of the periphery of 3D NAND and cross point memory is also provided.

What's After NAND?

In the near future, floating gate NAND flash is likely to encounter fundamental scaling limitations. A variety of technologies including Toshiba's BiCs, Samsung's VG-NAND, Macronix's BE-SONOS, SanDisk's 3D Memory (RRAM) and Intel/Micron's PCMs (stackable PCM) offer the promise of continued increases in storage capacities and lower cost per bit necessary to enable new and emerging data storage applications.

What's After NAND? provides an in-depth analysis of the post-floating gate NAND flash options and an independent assessment of the viability of these technologies going forward...

Applications for 3-bit per cell/4-bit per cell NAND Flash Memories

This report provides an in-depth analysis of the technology, performance, cost, market and applications for 3-bit per cell and 4-bit per cell NAND flash memories.

Solid State Drive Technology and Applications: A Primer

Solid State Drive Technology and Applications: A Primer is an ideal guide for novices interested in acquiring a basic understanding of SSD technology and applications as well as a handy reference for more experienced professionals. The report provides a detailed overview of the technology, architecture and reliability of SSDs as well as techniques for improving the performance and endurance. The advantages and disadvantages of SSDs versus HDDs in PCs and enterprise computing are examined along with an analysis of enterprise applications appropriate for SSD technology. The report also provides an overview of the competitive landscape for SSDs and relevant industry standards.

SSD Innovations

The unprecedented cost reductions of NAND flash memories in the last few years have driven 35mm film and 1.4" floppy disk to extinction. These first generation storage systems such as SD cards and USB flash drives are primarily removable, low capacity, low cost storage for consumer media.

The next frontier for NAND flash memory is as a hard disk drive replacement or an additional tier in the storage hierarchy. The traditional focus on performance in computing and storage farms now encompasses power savings and green technologies. The main reason is not only due to

environmental concerns but also to reduce the Total Cost of Ownership that is heavily impacted by electricity and cooling costs.

The priorities for solid state storage in the computing environment are dramatically different from those for consumer applications resulting in a new approach in the design of the system architecture. These varying requirements are driven by the different workload and environmental conditions. To satisfy these conditions, the type of memory used – SLC versus MLC – and system level management of wear leveling, garbage collection, FTL, ECC and security are key design considerations.

SSD Innovations focuses on innovative solutions from major industry players such as FusionIO, Intel, Pliant, Sandforce, SanDisk and STEC for improving the performance, endurance and reliability of SSDs. An exploration of the evolution of application requirements in computing applications, performance limitations of flash-based storage systems, trends and industry innovations is provided.

In addition, innovative SSD architectures incorporating new memory technologies, external power supply and linked chain architectures are investigated as future SSD development directions.

Phase Change Memory: Mainstream Ambitions

Phase Change Memory: Mainstream Ambitions outlines the challenges PCM faces as it vies to compete with mainstream charge-based memories. The report examines the feasilbility of PCM as a replacement for mainstream semiconductor memories including NOR flash, DRAM and NAND flash and explores the potential of PCM as a storage class memory. An update on the PCM activities of major vendors as well as a market and price forecast based on a detailed roadmap is also provided.

Graphics DRAM

The market for graphics DRAM is currently in a stage of massive changes.

In 2008, the market was well structured with only three of the main DRAM suppliers engaged in this market segment, namely Samsung, Hynix and Qimonda with a combined market share of greater than 90%. However, Qimonda's insolvency in January 2009 has disrupted this oligopoly. In May, Micron announced its intention to enter the Graphics DRAM market, followed by Elpida in August. Both companies managed to acquire know-how from the leftover Qimonda assets. Nevertheless, it will be a challenge for both newcomers to establish themselves in the graphics DRAM market.

This report analyzes the current status of the graphics DRAM market and provides an outlook for the following years.

In the first section, the market for GPUs and related graphics card platforms which is dominated by AMD and nVidia is discussed. An overview of the characteristics of different application segments as well as the current platforms of the two market leaders is provided.

The major part of this report analyses the market for graphics DRAM till 2012. This will include a detailed assessment of the memory I/Os and densities needed with forecasts for bit growth rates and memory speed requirements. An ASP and revenue forecast will be presented as well.

The last section focuses on the competitive situation in the graphics DRAM market. A thorough analysis of the competitive landscape and the competitiveness of the four players is provided. This discussion will be based on the market picture gained in the first two sections and the expected product portfolio and technology roadmaps of the various suppliers.

Key NAND Flash Memory Design Intellectual Property

Technical innovations, particularly in NAND flash memory design are key enablers of multi-level cell NAND flash memories, especially 3-bit per cell and 4-bit per cell technologies. This report identifies important intellectual property related to sensing architectures, source voltage noise compensation, programming algorithms, disturbs reduction, temperature compensation, high voltage switch, coding schemes and error correction codes from Hynix, Micron, Samsung, SanDisk, STMicroelectronics and Toshiba.

Comparison of 3-bit per cell NAND Flash Memories

This report compares the 3-bit per cell NAND flash memory architectures of SanDisk/Toshiba, Hynix and Samsung and analyzes the advantages and disadvantages of each implementation.

Read Architectures for 3-bit and 4-bit per cell NAND Flash Memories

This report explores the theory, basic circuit elements, timings, and key design features of the conventional interleaved architecture versus the all bitline sensing architecture.

Emerging Memories Technologies

Sometime in the next decade, both DRAM and flash memories are expected to face fundamental scaling limitations.

In DRAM, new device structures will be required to overcome short channel effects and junction leakage in the array transistor. In order to maintain the capacitor capacitance of 25fF, high aspect ratio structures and new high-k materials will be required as DRAM scales to 30nm.

NOR flash memory faces challenges in channel length scaling and maintaining the drain bias voltage margin necessary to minimize program disturb.

Electrostatic interference between adjacent cells in NAND flash is becoming a serious issue. As geometries shrink, it becomes much more difficult for the ONO dielectric to wrap around the floating gate to maintain the coupling ratio between the control gate and floating gate. Low-k materials

between the cells and high-k materials in the cell will be required for future generations of NAND flash.

As a consequence, DRAM and flash memory vendors are actively researching alternative memory technologies to ensure the continuation of Moore's Law. Technologies such as floating body cell memory and spin-torque MRAM offer the promise of non-volatile RAM-like performance.

Various technologies including phase change memory, charge trap memory, nanocrystal memory, PMC, RRAM and 3D memory are potential candidates to replace flash memory.

Emerging Memory Technologies provides an overview of the challenges facing emerging memory technologies as well as an analysis of the most likely memories to be commercialized in the next five years.