How 3D Memory Stacks Up

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Introduction

Mainstream NAND flash memories are currently manufactured on 4xnm processes with major NAND flash vendors migrating to 3xnm this year. In the race to reduce costs, NAND flash manufacturers are developing 2xnm technology, however with performance and reliability characteristics severely degraded relative to the 4xnm generation, 2xnm floating gate NAND flash could be the last process technology generation. What's next?

NAND flash vendors are actively exploring a variety of alternatives including spin-torque MRAM, nanocrystal memory, phase change memory and resistive memory. However as lithographic scaling becomes more challenging, companies are turning their sights to vertically stacked implementations of memory cells or 3D memory. 3D memory technologies offer the promise of continued increases in storage capacities and lower cost per bit necessary to enable emerging applications such as solid state drives.

Among the candidates: stacked NAND technologies employing charge trapping technology, vertical memory cells etched in a pillar and stackable cross-point memory arrays. This report explores the feasibility of each of these alternatives as a candidate to replace NAND flash memories within the next four years.

About the Authors

Josef Willer is Vice President of Technology. His expertise lies in the area of semiconductor memories including DRAM, NOR, NAND, NROM and alternative memory technologies including FRAM, MRAM, RRAM, phase change memory, nanocrystal memory, SONOS memory, spin-torque RAM and probe memory and the related intellectual property.

Josef brings with him a wealth of research and development experience in semiconductor memories from 26 years at Siemens Semiconductor / Infineon Technologies / Qimonda AG. Prior to joining Forward Insights, Josef was a principal at Qimonda Flash GmbH responsible for evaluating patents and intellectual property and developing innovative non-volatile memory technology and novel cell concepts to overcome the ultimate technology scaling constraints. Josef was instrumental in enabling the start-up company Ingentix to successfully demonstrate the feasibility of charge trapping technology for mass storage products.

In addition to his technical publications, Josef holds numerous memory-related patents and was named Infineon's Inventor of the Year in 2004. He has been a member of the technical committee of the ICMTD (International Conference on Memory Technology and Design) for the past three years.

Josef holds a Dr. rer. nat. from the Technical University in Munich in solid state physics.

Gregory Wong is the Founder and Principal Analyst. Greg has in-depth knowledge of the cost, performance and markets and applications of 2-bit per cell NOR, NROMand NAND flash, 3-bit per cell and 4-bit per cell NAND and 4-bit per cell NROM flash technologies as well as solid state drives. Greg has authored a variety of reports pertaining to the technology, performance, costs, markets and applications of flash and alternative non-volatile memories, solid state drives, 3-bit and 4-bit per cell NAND flash memories, flash cards and removable storage, and embedded flash memories. He also tracks wafer capacity and shipments by vendor and issues quarterly supply-demand and capex forecasts.

Greg has 11 years of management experience in strategic planning, business development and engineering at Hitachi, Siemens, ProMOS and Qimonda/Infineon. In these positions, Greg was responsible for analyzing and evaluating flash memory vendors' strategies, process technologies, design architectures, product performance, manufacturing capabilities and costs. Greg worked closely with senior management on strategy formulation and setting operational performance targets. He has worked in Canada, Japan, China, Taiwan and Germany.

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