Key NAND Flash Memory Design Intellectual Property

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Contents

List of Figures

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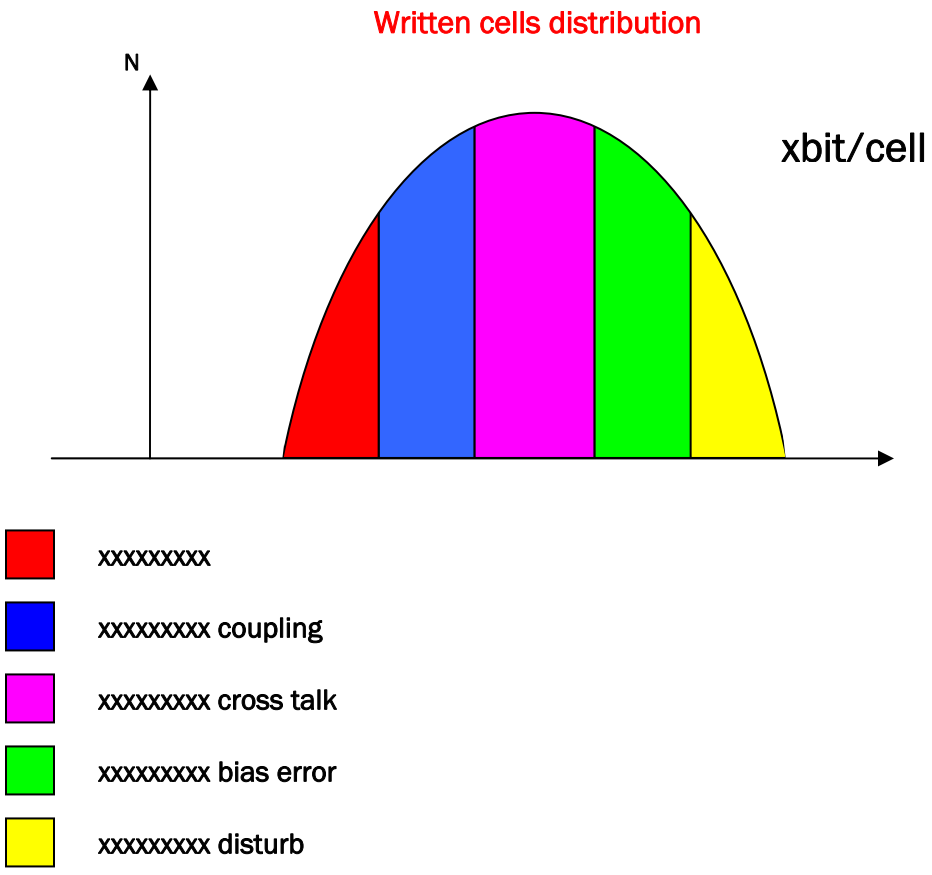
Sensing Architecture for Multi-state Memories

Figure 5 illustrates the most important contributors affecting the width of a programmed distribution. It is clear that in a multistate memory (3-4 bit/cells), it is important to reduce each single contributor otherwise there will be not enough space for all the seven (3bit/cell) or fifteen (4bit/cell) distributions inside the threshold voltage window.

Figure 5 NAND programmed distribution width: Contributors



The following is a collection of the most relevant and innovative patents, starting from the xxxxxxxxxx that replaced xxxxxxxxxx.

The advantages are explained in the next four patents: they differ from each other only for the claims (this is the reason why they are grouped in one analysis), strictly related to the patent's title.

They are fundamental from the point of view of design architecture and introduce the concept of xxxxxxxxxxxxxxxxxxx.

U.S. Patent No.xxxxxxxxxxxx

U.S. Patent No.xxxxxxxxxxxx

U.S. Patent No.xxxxxxxxxxxx

U.S. Patent No.xxxxxxxxxxxx
Inventors: xxxxxxxxxxxxx
Assignee: **xxxxxxxxxxxxx**

Analysis

These patents contain the novel concept of the xxxxxxxxx, sensing and program, and the source bias error reduction algorithm. It is important to note, as claimed in Patent No. xxxxxxxx the wide spectrum of memory covered under these patents: EEPROM NROM and Flash EEPROM, NAND/NOR architecture with floating gate or charge trapping cells type.

The patents are generic concepts relatively easy to implement and applicable to different non-volatile memories. No prior art is present for xxxxxxxxx. It is not easy to find a workaround on these patents. The major claims are related to:

- xxxxxx biasing independent of time

- xxxxxxxx at xxxxxxx

- xxxxxxxx

- generic algorithm for xxxxxxxx

- use of a dedicated xxxxxxx inside xxxxxxx for xxxxxxxx

xxxxxxxx is mandatory for a competitive a multistate memory - the advantages are enormous compared to the xxxxxxx architecture and is primarily implemented in the latest multistate xxxxxx NAND memory generations:

- xxxxxxxx

- xxxxxxxx

- xxxxxxxx

SUMMARY OF INVENTION

The need for a high capacity and high performance non-volatile memory device are met by having a large page of read/write circuits to read and write a corresponding page of memory cells in parallel. In particular, xxxxxxxxxxxxxx inherent in high density chip integration that may introduce errors into reading and programming are either ***eliminated or minimized.***

Here are the highlights:

- xxxxxxxxx is eliminated

- xxxxxxxxx is strongly reduced and theoretically, with a certain number of loops eliminated

- xxxxxxxxx is reduced

- xxxxxxxxx is reduced (halved)

The following is a brief description of xxxxxxxxx and how it is reduced.

xx

About the Author

Luca Crippa is Senior Technical Analyst for Design Architecture. Luca has more than 10 years of experience in **MLC flash memory design**. Previously, he was Senior Designer for 48nm floating gate and 36nm floating gate NAND flash memories at Qimonda AG as well as 90nm and 60nm MLC NAND flash products at STMicroelectronics.

He was instrumental in the development of 64Mb, 128Mb and 256Mb MLC NOR flash products at STMicroelectronics and is the author/co-author of 20 U.S. patents and the book *Memories in Wireless Systems* (Springer-Verlag ed., 2008).

Luca received his Bachelors degree at ITIS G. Marconi, Dalmine, Italy in 1992 and a Masters degree in Electronic Engineering at the Politecnico of Milan in 1999. His thesis topic was *Analog circuits design for Multilevel Flash Memory*.

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