



Read Architectures for Multi-bit per cell NAND Flash Memories

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3-bit per cell/4-bit per cell NAND Flash Memories

An in-depth analysis of the technology, performance, cost, market and applications for 3-bit per cell and 4-bit per cell NAND flash memories.

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Technical innovations, particularly in NAND flash memory design are key enablers of multi-level cell NAND flash memories, especially 3-bit per cell and 4-bit per cell technologies. This report identifies important intellectual property related to sensing architectures, source voltage noise compensation, programming algorithms, disturbs reduction, temperature compensation, high voltage switch, coding schemes and error correction codes from Hynix, Micron, Samsung, SanDisk, STMicroelectronics and Toshiba.

Read Architectures for Multi-bit per cell NAND Flash Memories

Compares the technical merits of the All Bitline sensing architecture vs. conventional voltage sensing scheme in NAND flash memories.

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Explores the various ECC techniques used in NAND flash memories including BCH, RS as well as emerging DSP coding techniques. DSP coding techniques will be essential for implementing 3-bit and 4-bit per cell NAND flash memories and future generations of NAND flash in solid state drives.

Comparison of 3-bit per cell NAND Flash Memories

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