Read Architectures for Multi-bit per cell NAND Flash Memories

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About the Author

Luca Crippa is Senior Technical Analyst for Design Architecture. Luca has more than 10 years of experience in **MLC flash memory design**. Previously, he was Senior Designer for 48nm floating gate and 36nm floating gate NAND flash memories at Qimonda AG as well as 90nm and 60nm MLC NAND flash products at STMicroelectronics.

He was instrumental in the development of 64Mb, 128Mb and 256Mb MLC NOR flash products at STMicroelectronics and is the author/co-author of 20 U.S. patents and the book *Memories in Wireless Systems* (Springer-Verlag ed., 2008).

Luca received his Bachelors degree at ITIS G. Marconi, Dalmine, Italy in 1992 and a Masters degree in Electronic Engineering at the Politecnico of Milan in 1999. His thesis topic was *Analog circuits design for Multilevel Flash Memory*.

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Compares the technology, challenges and cost of various 3D memory options including stacked charge trapping technologies from Samsung and Toshiba, and cross-point RRAM arrays.

NAND Quarterly Insights
A quarterly supply-demand forecast published four times a year which includes vendor shipments, wafer capacity, capex, and application forecasts. The report also contains roadmaps and costs for SLC, MLC, 3-bit/cell and 4-bit/cell technologies.

3-bit per cell/4-bit per cell NAND Flash Memories
An in-depth analysis of the technology, performance, cost, market and applications for 3-bit per cell and 4-bit per cell NAND flash memories.

Key NAND Flash Memory Design Intellectual Property
Technical innovations, particularly in NAND flash memory design are key enablers of multi-level cell NAND flash memories, especially 3-bit per cell and 4-bit per cell technologies. This report identifies important intellectual property related to sensing architectures, source voltage noise compensation, programming algorithms, disturbs reduction, temperature compensation, high voltage switch, coding schemes and error correction codes from Hynix, Micron, Samsung, SanDisk, STMicroelectronics and Toshiba.

Read Architectures for Multi-bit per cell NAND Flash Memories
Compares the technical merits of the All Bitline sensing architecture vs. conventional voltage sensing scheme in NAND flash memories.

Solid State Drives
Provides an overview of the technology, performance, cost trends and market and application forecasts of solid state drives in computing applications.

ECC and Signal Processing Technology for Solid State Drives and Multi-bit per cell Flash Memories
Explores the various ECC techniques used in NAND flash memories including BCH, RS as well as emerging DSP coding techniques. DSP coding techniques will be essential for implementing 3-bit and 4-bit per cell NAND flash memories and future generations of NAND flash in solid state drives.

Comparison of 3-bit per cell NAND Flash Memories
This report compares the 3-bit per cell NAND flash memory implementations of SanDisk/Toshiba, Hynix and Samsung and discusses the advantages and disadvantages of each.

SSD Innovations
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